FIG 1

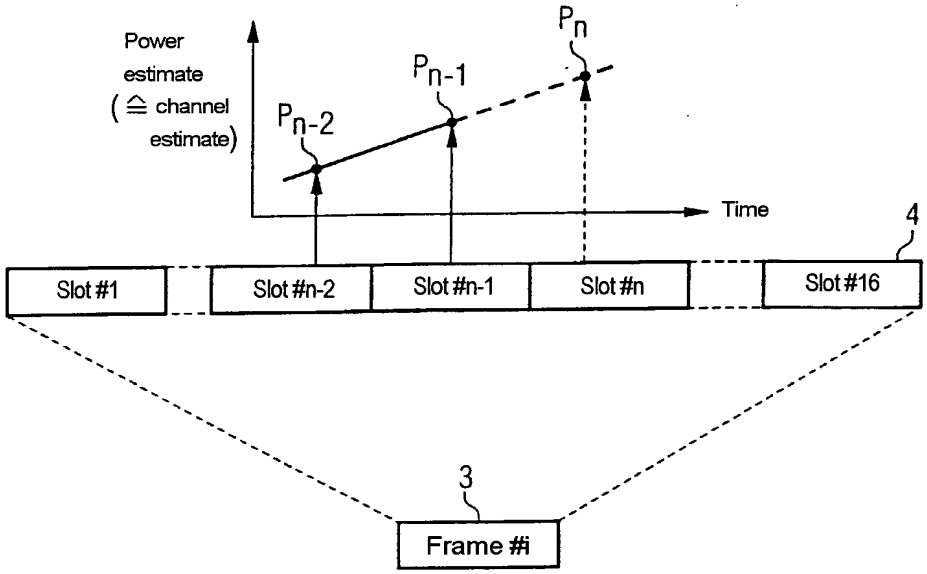

Power
estimate
(≙ channel
estimate)
P_{n-2}
P_{n-1}
P_n
Time
4
Slot #1
Slot #n-2
Slot #n-1
Slot #n
Slot #16
3
Frame #i

FIG 2

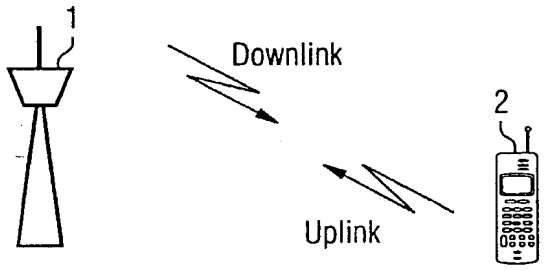
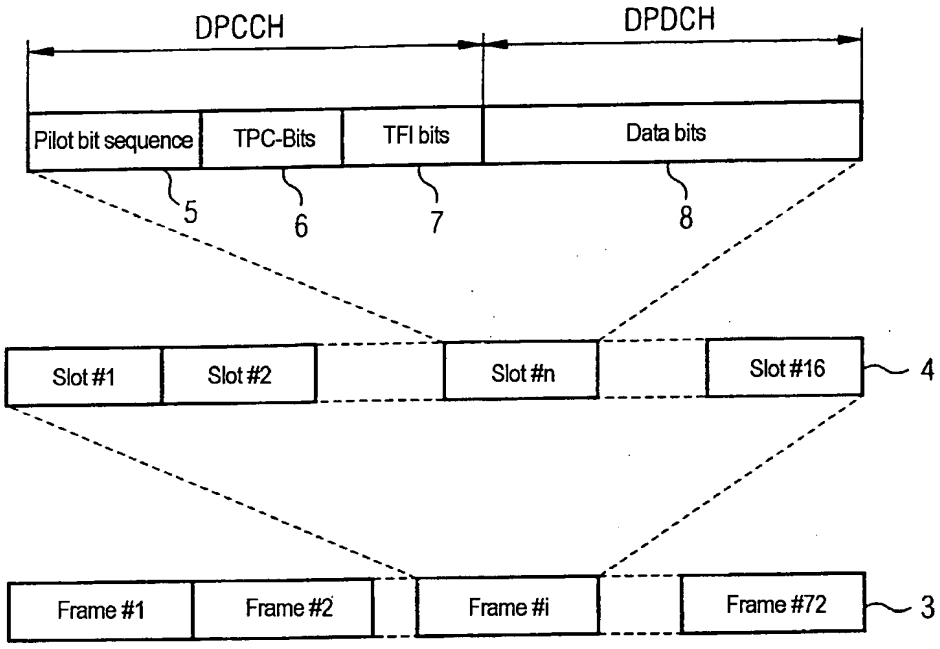

1
Downlink
2
Uplink

FIG 3



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